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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,449	HEITKAMP ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *12 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20 and 21* is/are allowed.

6)☒ Claim(s) *1-19,22,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,526,464 to Jobs et al. ("Jobs"), US Patent Number 6,381,239 to Atkinson et al. ("Atkinson"), and US Patent Number 5,957,985 to Wong et al. ("Wong").

3. In reference to Claim 1, Jobs teaches a master control processor (See Figure 2 Number 240); a bus controller connected to the processor that implements a serial bus interface between the processor and a plurality of serial bus devices (See Figure 2 Number 202); and a switch configured to electrically connect the circuit board corresponding to the switch to the first circuit board through the serial bus interface when the switch is controlled to be in a first state and to electrically isolate the circuit board corresponding to the switch from the serial bus interface on the first circuit board when the switch is controlled to be in a second state (See Figure 2 Numbers 206 and 208). Jobs does not teach the processor and bus controller being on a first circuit

board; a midplane connected to the bus controller on the first circuit board; a plurality of additional circuit boards connected to the serial bus interface through the midplane; each additional board including one or more of the serial bus devices; local control logic for outputting a signal for controlling the state of the switch; and the local control logic controlling the switch to be in the first state when the switches on each of the other of the plurality of additional circuit boards are in the second state. Atkinson teaches a computer device containing a midplane which has a plurality of cards connected to it (See Figure 1 Number 1, and Column 9 Lines 12-15); a serial message bus connecting the cards across the midplane (See Figure 1 Number 9); and a processor and bus interface on a first circuit board (See Figure 1 Numbers 44, 46, and 48). Wong teaches intelligent components (analogous to the switches) that have a local controller (analogous to the local control logic) for operating the component, said intelligent components connected to a bus which is further connected to a master control unit (See Figures 1, 3, and 6, Column 3 Lines 58-67, and Column 4 Lines 1-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs with the plurality of cards containing a processor and bus interface connected through a midplane containing a serial bus of Atkinson and the local control logic of Wong, resulting in the invention of Claim 1, in order to construct the serial bus of Jobs with an open architecture that readily accommodates insertion of newly designed hardware and/or software (See Column 6 Lines 6-10 of Atkinson); and to provide a level of redundancy by allowing the local control logic to control the switches and using the master control unit to control the

switch if the local control logic fails (See Column 4 Lines 27-29 and Column 5 Lines 16-26 of Wong).

4. In reference to Claim 2, Jobs, Atkinson, and Wong teach the limitations as applied to Claim 1 above. Jobs further teaches basic input-output routines in NVRAM (analogous to the master control logic) connected to the master control processor to control the gates (See Figure 2 Number 228 and Column 2 Lines 46-49). Wong further teaches that the local controller is under the control of a master controller (analogous to the master control logic) (See Column 4 Lines 21-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs with the plurality of cards containing a processor and bus interface connected through a midplane containing a serial bus of Atkinson and the local control logic of Wong, resulting in the invention of Claim 2, in order to construct the serial bus of Jobs with an open architecture that readily accommodates insertion of newly designed hardware and/or software (See Column 6 Lines 6-10 of Atkinson); and to provide a level of redundancy by allowing the local control logic to control the switches and using the master control unit to control the switch if the local control logic fails (See Column 4 Lines 27-29 and Column 5 Lines 16-26 of Wong).

5. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, and Wong as applied to Claim 2 above, and further in view of US Patent Number 6,301,623 to Simpson et al ("Simpson").

6. In reference to Claim 3, Jobs, Atkinson, and Wong teach the limitations as in Claim 2 above. Jobs, Atkinson, and Wong do not teach a multiplexer connected to the output of the bus controller and dividing the serial bus interface into a plurality of sub-buses, only one of which is connected to the bus controller by the multiplexer at any given time. Simpson teaches the use of a multiplexer to divide a serial channel into a plurality of device groups, only one of which is accessible at a time (See Abstract, Figure 4, Column 1, Lines 66-67, and Column 2, Lines 1-15 of Simpson).

It would have been obvious to one of ordinary skill in the art at the time the invention was made would combine the device of Jobs, Atkinson, and Wong with the device of Simpson, resulting in the invention of Claim 3, in order to allow virtually limitless expansion of the address space (See Column 2, Lines 58-63 of Simpson).

7. In reference to Claim 6, Jobs, Atkinson, Wong, and Simpson teach the limitations as in Claim 3 above. Jobs, Atkinson, and Wong do not teach one of the sub-buses being connected to the plurality of additional circuit boards. Simpson further teaches that a plurality of stations (analogous to the circuit boards) can be connected to each sub-bus through the communication module (See Figure 2 and Column 3 Lines 60-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made would combine the device of Jobs, Atkinson, and Wong with the device of Simpson, resulting in the invention of Claim 6, in order to allow virtually limitless expansion of the address space (See Column 2, Lines 58-63 of Simpson).

8. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, Wong, and Simpson as applied to Claim 3 above, and further in view of US Patent Number 6,532,500 to Li et al. ("Li") and US Patent Number 6,122,756 to Baxter et al. ("Baxter").

9. In reference to Claim 4, Jobs, Atkinson, Wong, and Simpson teach the limitations as in Claim 3 above. Jobs, Atkinson, Wong, and Simpson do not teach the serial bus devices including at least one of a temperature sensor, a voltage monitor, and an ID EPROM. Li teaches a serial temperature sensor and a serial voltage sensor (See Column 4 Lines 23-49). Baxter teaches an ID EPROM device (See Figure 2 Number 204).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs, Atkinson, Wong, and Simpson, with the temperature and voltage sensors of Li and the ID EPROM of Baxter, resulting in the invention of Claim 4, in order to provide signals representing the operating parameters of various devices in the computer system such as temperature and voltage (See

Column 4 Lines 23-26 and Column 4 Lines 30-33 of Li); and provide a non-volatile way to store important system information (See Column 11 Lines 42-44 of Baxter).

10. In reference to Claim 5, Jobs, Atkinson, Wong, and Simpson teach the limitations as in Claim 3 above. Jobs, Atkinson, Wong, and Simpson do not teach one of the serial bus devices including an ID EPROM connected to the midplane. Baxter teaches a system ID SEEPROM (Serial EEPROM) device located on the backpanel (analogous to the midplane) (See Column 10 Lines 27-29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs, Atkinson, Wong, and Simpson with the temperature and voltage sensors of Li and the midplane-mounted ID SEEPROM of Baxter, resulting in the invention of Claim 5, in order to provide signals representing the operating parameters of various devices in the computer system such as temperature and voltage (See Column 4 Lines 23-26 and Column 4 Lines 30-33 of Li); and provide a non-volatile way to store important system information (See Column 11 Lines 42-44 of Baxter).

11. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, and Wong as applied to Claim 1 above, and further in view of US Patent Number 4,845,736 to Posner et al. ("Posner").

12. In reference to Claim 7, Jobs, Atkinson, and Wong teach the limitations as in to Claim 1 above. Jobs, Atkinson, and Wong do not teach a first switch for selectively connecting or disconnecting a first portion of a serial bus, implemented by the serial bus interface from the first circuit board, to a second portion of the serial bus; a second switch for selectively connecting or disconnecting the second portion of the serial bus to a third portion of the serial bus; and a third switch for selectively connecting or disconnecting the third portion of the serial bus to a fourth portion of the serial bus. Posner teaches a plurality of cross connect switches that can have any number of inputs and outputs (See Figure 11 and Column 1 Lines 38-41); wherein the input (analogous to the first portion of the serial bus) is connected to the first switch, the first switch has a connection to the second switch (analogous to the second portion of the serial bus), the second switch has a connection to the third switch (analogous to the third portion of the serial bus), and the third switch is connected to the output (analogous to the fourth portion of the serial bus) (See Figure 11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs, Atkinson, and Wong with the switches of Posner, resulting in the invention of Claim 7, in order to allow the second portion of the bus to be connected to different first portions of the bus, the third portion of the bus to be connected to different second portions of the bus, and the fourth portion of the bus to be connected to different third portions of the bus (See Column 1 Lines 14-17 and Column 14 Lines 45-53 of Posner); and to reduce the capacitive loading of the

devices on the bus by disconnecting segments not in use, since it is known in the art that capacitive loading degrades performance.

13. In reference to Claim 8, Jobs, Atkinson, Wong, and Posner teach the limitations as in Claim 7 above. Atkinson further teaches an application processor (analogous to the local processor) connected to the serial bus through a communication processor (analogous to the bus controller) (See Figure 1 Numbers 9, 12, and 16). Posner further teaches a computer (analogous to the local control logic) that is used to control the first, second, and third switches (See Figure 11 Number 422 and Column 15 Lines 33-34).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs, Atkinson, and Wong with the switches and controller of Posner, resulting in the invention of Claim 8, in order to control board specific processing (See Column 17 Lines 43-45 of Atkinson); to facilitate communications between cards (See Column 17 Lines 50-52 of Atkinson); to provide each card with the necessary processing resources (See Column 17 Lines 32-35 of Atkinson); to allow the second portion of the bus to be connected to different first portions of the bus, the third portion of the bus to be connected to different second portions of the bus, and the fourth portion of the bus to be connected to different third portions of the bus (See Column 1 Lines 14-17 and Column 14 Lines 45-53 of Posner); and to reduce the capacitive loading of the devices on the bus by disconnecting segments not in use, since it is known in the art that capacitive loading degrades performance.

14. Claims 9, 10, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, and US Patent Number 6,330,614 to Aggarwal et al. ("Aggarwal").

15. In reference to Claim 9, Jobs teaches a device (analogous to the packet forwarding engine) comprising a first circuit board having a master control processor (See Figure 2 Number 240); and a plurality of switches configured to electrically connect a serial bus to the first circuit board when the switch is controlled to be in a first state and to electrically isolate the serial bus from the first circuit board when the switch is controlled to be in a second state, wherein the switch of a particular serial bus being in the first state only when the switches for each of the other serial busses are in the second state (See Figure 2 Numbers 206 and 208 and Column 2 Lines 26-39). Jobs does not teach a routing engine for consolidating routing information learned from routing protocols in the network; the packet forwarding engine including a midplane; and a plurality of second circuit boards each having a control processor. Aggarwal teaches a routing engine (See Figures 3 and 4, Column 4, Lines 34-38, and Column 5, Lines 49-66 of Aggarwal). Atkinson teaches a computer device containing a midplane which has a plurality of cards connected to it (See Figure 1 Number 1, and Column 9 Lines 12-15); a serial message bus connecting the cards across the midplane (See Figure 1 Number 9); a processor and bus interface on a first circuit board (See Figure 1 Numbers 44, 46, and 48); and a control processor on each of the second circuit boards (See Figure 1 Number 12).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs with the routing engine of Aggarwal and the plurality of cards containing a processor and bus interface connected through a midplane containing a serial bus of Atkinson, resulting in the invention of Claim 9, in order to construct the serial bus of Jobs with an open architecture that readily accommodates insertion of newly designed hardware and/or software (See Column 6 Lines 6-10 of Atkinson); to control board specific processing (See Column 17 Lines 43-45 of Atkinson); to facilitate communications between cards (See Column 17 Lines 50-52 of Atkinson); to provide each card with the necessary processing resources (See Column 17 Lines 32-35 of Atkinson); and to create a forwarding table allowing the device to determine the proper output port based on the destination address of incoming packets (See Column 6 Lines 4-48 of Aggarwal).

16. In reference to Claim 10, Jobs, Atkinson, and Aggarwal teach the limitations as in Claim 9 above. Aggarwal further teaches that the network device is a network router (See Figures 3 and 4, Column 2 Lines 26-42, and Column 5, Lines 49-66).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs with the routing engine of Aggarwal and the plurality of cards containing a processor and bus interface connected through a midplane containing a serial bus of Atkinson, resulting in the invention of Claim 10, in order to construct the serial bus of Jobs with an open architecture that readily accommodates insertion of newly designed hardware and/or software (See Column 6

Lines 6-10 of Atkinson); to control board specific processing (See Column 17 Lines 43-45 of Atkinson); to facilitate communications between cards (See Column 17 Lines 50-52 of Atkinson); to provide each card with the necessary processing resources (See Column 17 Lines 32-35 of Atkinson); and to create a forwarding table allowing the device to determine the proper output port based on the destination address of incoming packets (See Column 6 Lines 4-48 of Aggarwal).

17. In reference to Claim 13, Jobs, Atkinson, and Aggarwal teach the limitations as applied to Claim 9 above. Jobs further teaches a bus controller connected to the processor that implements a serial bus interface between the processor and a plurality of serial bus devices (See Figure 2 Number 202).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs with the routing engine of Aggarwal and the plurality of cards containing a processor and bus interface connected through a midplane containing a serial bus of Atkinson, resulting in the invention of Claim 9, in order to construct the serial bus of Jobs with an open architecture that readily accommodates insertion of newly designed hardware and/or software (See Column 6 Lines 6-10 of Atkinson); to control board specific processing (See Column 17 Lines 43-45 of Atkinson); to facilitate communications between cards (See Column 17 Lines 50-52 of Atkinson); to provide each card with the necessary processing resources (See Column 17 Lines 32-35 of Atkinson); and to create a forwarding table allowing the

device to determine the proper output port based on the destination address of incoming packets (See Column 6 Lines 4-48 of Aggarwal).

18. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, and Aggarwal as applied to Claim 9 above, and further in view of Wong.

19. In reference to Claim 11, Jobs, Atkinson, and Aggarwal teach the limitations as in Claim 9 above. Jobs, Atkinson, and Aggarwal do not teach local control logic coupled to receive control information from the master control processor and the control processor corresponding to the second circuit board of the local control logic; and the local control logic controlling the switch to be in the first or second state based on the received control information. Wong teaches intelligent components (analogous to the switches) that have a local controller (analogous to the local control logic) for operating the component, said intelligent components connected to a bus which is further connected to a master control unit (See Figures 1, 3, and 6, Column 3 Lines 58-67, and Column 4 Lines 1-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs and Atkinson with the local control logic of Wong, resulting in the invention of Claim 11, in order to provide a level of redundancy by allowing the local control logic to control the switches and using the

master control unit to control the switch if the local control logic fails (See Column 4 Lines 27-29 and Column 5 Lines 16-26 of Wong).

20. In reference to Claim 12, Jobs, Atkinson, Aggarwal, and Wong teach the limitations as applied to Claim 11 above. Jobs further teaches basic input-output routines in NVRAM (analogous to the master control logic) connected to the master control processor to control the gates (See Figure 2 Number 228 and Column 2 Lines 46-49). Wong further teaches that the local controller is under the control of a master controller (analogous to the master control logic) (See Column 4 Lines 21-31).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs, Atkinson, and Aggarwal with the local control logic of Wong, resulting in the invention of Claim 12, in order to construct the serial bus of Jobs with an open architecture that readily accommodates insertion of newly designed hardware and/or software (See Column 6 Lines 6-10 of Atkinson); and to provide a level of redundancy by allowing the local control logic to control the switches and using the master control unit to control the switch if the local control logic fails (See Column 4 Lines 27-29 and Column 5 Lines 16-26 of Wong).

21. Claims 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, and Aggarwal as applied to Claim 13 above, and further in view of Simpson.

22. In reference to Claim 14, Jobs, Atkinson, and Aggarwal teach the limitations as in Claim 13 above. Jobs, Atkinson, and Aggarwal do not teach a multiplexer connected to the output of the bus controller and dividing the serial bus interface into a plurality of sub-buses, only one of which is connected to the bus controller by the multiplexer at any given time. Simpson teaches the use of a multiplexer to divide a serial channel into a plurality of device groups, only one of which is accessible at a time (See Abstract, Figure 4, Column 1, Lines 66-67, and Column 2, Lines 1-15 of Simpson).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs, Atkinson, and Aggarwal with the device of Simpson, resulting in the invention of Claim 14, in order to allow virtually limitless expansion of the address space (See Column 2, Lines 58-63 of Simpson).

23. In reference to Claim 17, Jobs, Atkinson, Aggarwal, and Simpson teach the limits as applied to Claim 14 above. Atkinson further teaches a serial bus that is connected to a plurality of circuit boards (See Figure 1 Number 9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs, Atkinson, and Aggarwal with the device of Simpson, resulting in the inventions of Claim 17, in order to allow virtually limitless expansion of the address space (See Column 2, Lines 58-63 of Simpson).

24. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jobs, Atkinson, Aggarwal, and Simpson as applied to Claim 14 above, and further in view of Li and Baxter.

25. In reference to Claim 15, Jobs, Atkinson, Aggarwal, and Simpson teach the limitations as in Claim 14 above. Jobs, Atkinson, Aggarwal, and Simpson do not teach the serial bus devices including at least one of a temperature sensor, a voltage monitor, and an ID EPROM. Li teaches a serial temperature sensor and a serial voltage sensor (See Column 4 Lines 23-49 of Li). Baxter teaches an ID EPROM device (See Figure 2 Number 204).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs, Atkinson, Wong, and Simpson with the temperature and voltage sensors of Li and the ID EPROM of Baxter, resulting in the invention of Claim 15, in order to provide signals representing the operating parameters of various devices in the computer system such as temperature and voltage (See Column 4 Lines 23-26 and Column 4 Lines 30-33 of Li); and provide a non-volatile way to store important system information (See Column 11 Lines 42-44 of Baxter).

26. In reference to Claim 16, Jobs, Atkinson, Aggarwal, and Simpson teach the limitations as in Claim 14 above. Jobs, Atkinson, Aggarwal, and Simpson do not teach one of the serial bus devices including an ID EPROM connected to the midplane.

Baxter teaches a system ID SEEPROM (Serial EEPROM) device located on the backpanel (analogous to the midplane) (See Column 10 Lines 27-29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Jobs, Atkinson, Wong, and Simpson with the temperature and voltage sensors of Li and the midplane-mounted ID SEEPROM of Baxter, resulting in the invention of Claim 16, in order to provide signals representing the operating parameters of various devices in the computer system such as temperature and voltage (See Column 4 Lines 23-26 and Column 4 Lines 30-33 of Li); and provide a non-volatile way to store important system information (See Column 11 Lines 42-44 of Baxter).

27. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson, Posner and Wong.

28. In reference to Claim 18, Atkinson teaches an application processor (analogous to the local processor) on a circuit board connected to the serial bus through a communication processor (analogous to the bus controller) (See Figure 1 Numbers 9, 12, and 16). Atkinson does not teach a first switch for selectively connecting or disconnecting a first portion of a two wire serial bus from an external circuit board to a second portion of the two wire serial bus; a second switch for selectively connecting or disconnecting the second portion of the two wire serial bus to a third portion of the two wire serial bus; a third switch for selectively connecting or disconnecting the third

portion of the two wire serial bus to a fourth portion of the two wire serial bus; and a local control logic circuit connected to receive control information from the external circuit board and the local processor and control the first, second, and third switches based on the received control information. Posner teaches a plurality of cross connect switches that can have any number of inputs and outputs (See Figure 11 and Column 1 Lines 38-41); wherein the input (analogous to the first portion of the serial bus) is connected to the first switch, the first switch has a connection to the second switch (analogous to the second portion of the serial bus), the second switch has a connection to the third switch (analogous to the third portion of the serial bus), the third switch is connected to the output (analogous to the fourth portion of the serial bus) (See Figure 11); and local control logic that is used to control the first, second, and third switches (See Figure 11 Number 422 and Column 15 Lines 33-34). Wong teaches intelligent components (analogous to the switches) that have a local controller (analogous to the local control logic) for operating the component, said intelligent components connected to a bus which is further connected to a master control unit (See Figures 1, 3, and 6, Column 3 Lines 58-67, and Column 4 Lines 1-7) and can receive signals from the master controller (analogous to the external circuit board) and the sensor (analogous to the local processor) (See Figure 3 and Column 6 Lines 26-29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the circuit board, application processor, serial bus, and communication processor of Atkinson with the switches and controller of Posner, resulting in the invention of Claim 18, in order to allow the second portion of the bus to

be connected to different first portions of the bus, the third portion of the bus to be connected to different second portions of the bus, and the fourth portion of the bus to be connected to different third portions of the bus (See Column 1 Lines 14-17 and Column 14 Lines 45-53 of Posner); to reduce the capacitive loading of the devices on the bus by disconnecting segments not in use, since it is known in the art that capacitive loading degrades performance; and to provide a level of redundancy by allowing the local control logic to control the switches and using the master control unit to control the switch if the local control logic fails (See Column 4 Lines 27-29 and Column 5 Lines 16-26 of Wong).

29. In reference to Claim 19, Atkinson, Posner, and Wong teach the limitations as in Claim 18 above. Posner further teaches that the cross connect switch, under the control of the computer (analogous to the local control logic), can connect a specified input line (analogous to the external circuit board) to a specified output line (See Column 14 Lines 38-40). Since the computer can connect the input line to an output line not connected to the local processor, it inherently can connect the external circuit board and the local processor to different portions of the bus.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the circuit board, application processor, serial bus, and communication processor of Atkinson with the switches and controller of Posner, resulting in the invention of Claim 19, in order to allow the second portion of the bus to be connected to different first portions of the bus, the third portion of the bus to be

connected to different second portions of the bus, and the fourth portion of the bus to be connected to different third portions of the bus (See Column 1 Lines 14-17 and Column 14 Lines 45-53 of Posner); to reduce the capacitive loading of the devices on the bus by disconnecting segments not in use, since it is known in the art that capacitive loading degrades performance; and to provide a level of redundancy by allowing the local control logic to control the switches and using the master control unit to control the switch if the local control logic fails (See Column 4 Lines 27-29 and Column 5 Lines 16-26 of Wong).

30. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson, Posner, and Wong as applied to Claim 18 above, and further in view of US Patent Number 5,185,693 to Loftis et al. ("Loftis").

31. In reference to Claim 22, Atkinson, Posner, and Wong teach the limitations as in Claim 18 above. Atkinson, Posner, and Wong do not teach the local control logic controlling the first, second, and third switches so that if the first switch is disconnected, the second and third switches are controlled by the local processor. Loftis teaches a system of two processors, one of which is granted access to a series of I/O devices (analogous to switches 2 and 3) while the other is denied access based on the position of a switch (analogous to switch 1) (See Abstract, Figures 1 and 2, and Column 2 Lines 14-21).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Atkinson, Posner, and Wong with the switch controlled access of Loftis, resulting in the invention of Claim 22, in order to provide redundant control of the bus and switches in the event that the master controller is faulty (See Column 2 Lines 1-4 and Column 2 Lines 7-14 of Loftis).

32. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson, Posner, and Wong as applied to Claim 18 above, and further in view of Li.

33. In reference to Claim 24, Atkinson, Posner, and Wong teach the limitations as in Claim 18 above. Atkinson, Posner, and Wong do not teach at least one of a voltage monitor and a temperature sensor are connected to the second portion of the two wire serial bus. Li teaches a serial temperature sensor and a serial voltage sensor (See Figure 2 Number 142 and Column 4 Lines 23-49).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Atkinson, Posner, and Wong with the temperature and voltage sensors of Li, resulting in the invention of Claim 24, in order to provide signals representing the operating parameters of various devices connected to the second bus in the computer system such as temperature and voltage (See Column 4 Lines 23-26 and Column 4 Lines 30-33 of Li).

34. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Atkinson, Posner, and Wong as applied to Claim 18 above, and further in view of Baxter.

35. In reference to Claim 25, Atkinson, Posner, and Wong teach the limitations as in Claim 18 above. Atkinson, Posner, and Wong do not teach an ID EPROM connected to the third portion of the two wire serial bus. Baxter teaches an ID EPROM device (See Figure 2 Number 204).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Atkinson, Posner, and Wong with the ID EPROM of Baxter, resulting in the invention of Claim 25, in order to provide a non-volatile way to store important system information about the devices connected to the third bus portion (See Column 11 Lines 42-44 of Baxter).

Allowable Subject Matter

36. Claims 20 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The closest prior art that has been found is the combination of Atkinson, Posner, and Wong as applied to Claim 19 and the combination of Atkinson, Posner, Wong, and Loftis as applied to Claim 22. Neither of the aforementioned combinations teach that the local control logic circuit

controls the first, second, and third switches so that if the first and second switches are connected, the third switch is disconnected as in Claim 20; or that the local control logic circuit controls the first, second, and third switches so that if the first switch is connected and the second switch is disconnected, the third switch is connected. Further, no prior art or motivation has been found that would result in the all of the limitations of the aforementioned claims, either alone or in combination.

Response to Arguments

37. Applicant's arguments, see Pages 3-22, filed 12 February 2004, with respect to the rejections of Claims 1 and 2 over Jobs, Atkinson, and Buckley; Claims 3 and 6 over Jobs, Atkinson, Buckley, and Simpson; Claims 4 and 5 over Jobs, Atkinson, Buckley, Simpson, Li, and Baxter; Claims 7 and 8 over Jobs, Atkinson, Buckley, and Posner; Claims 11 and 12 over Jobs, Atkinson, Aggarwal, and Buckley; Claims 18 and 19 over Atkinson, Posner, and Buckley; Claim 22 over Atkinson, Posner, Buckley, and Loftis; Claim 24 over Atkinson, Posner, Buckley, and Li; and Claim 25 over Atkinson, Posner, Buckley, and Baxter have been fully considered and are persuasive. The aforementioned rejections of Claims 1-8, 11-12, 22, and 24-25 have been withdrawn.

38. Applicant's arguments filed 12 February 2004 with respect to the rejection of Claims 1 and 2 over Jobs, Atkinson, and Wong have been fully considered but they are not persuasive. Applicant has argued that Atkinson does not disclose that each circuit

board includes the switch recited in Claim 1. The Examiner is relying on Atkinson to teach a plurality of circuit boards each containing a serial sub bus connected together through a midplane, and Jobs to teach a switching device to provide access to a serial sub bus. Applicant has further argued that Wong does not disclose the switch and the local control logic recited in Claim 1. Wong teaches that a plurality of components, such as the switch of Jobs, can be connected to the primary bus, and that each component has a local controller (See Column 4 Lines 1-4). In response to Applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, as shown above, Atkinson provides a means to expand the serial bus of Jobs by using an open architecture that readily accommodates insertion of newly designed hardware and/or software (See Column 6 Lines 6-10 of Atkinson). In response to Applicant's argument that the motivation for combining Jobs and Atkinson with Wong are merely features/advantages of the system described by Wong, the Examiner notes that the motivation provided shows a benefit to using intelligent components having a local processor.

39. Applicant's arguments filed 12 February 2004 with respect to the rejection of Claims 3 and 4 over Jobs, Atkinson, Wong, and Simpson have been fully considered but they are not persuasive. Examiner notes that in the aforementioned rejections, Simpson is not being relied upon to teach elements of Claim 2.

40. Applicant's arguments filed 12 February 2004 with respect to the rejection of Claims 5 and 6 over Jobs, Atkinson, Wong, Simpson, Li, and Baxter have been fully considered but they are not persuasive. Examiner notes that in the aforementioned rejections, Li and Baxter are not being relied upon to teach elements of Claim 3.

41. Applicant's arguments filed 12 February 2004 with respect to the rejection of Claims 7 and 8 over Jobs, Atkinson, Wong, and Posner have been fully considered but they are not persuasive. Examiner notes that the switches of Posner, in addition to forming a complete link between an input and an output, also selectively connect and disconnect segments of the link (analogous to portions of the serial bus). Further, the switches of Posner, when creating a link between two segments, selectively selects those segments, and when not creating a link between two segments, selectively disconnects those segments.

42. Applicant's arguments filed 12 February 2004 with respect to the rejection of Claims 9, 10, and 13 over Jobs, Atkinson, and Aggarwal have been fully considered but they are not persuasive. Examiner notes that when Jobs and Atkinson are combined as

described above, the switches would be included on a plurality of circuit boards and connected as recited in Claim 9. In response to Applicant's argument that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). The Examiner notes that, as shown in the above rejections, the motivation provided to use Atkinson teaches a benefit to using the features of Atkinson (a midplane which has a plurality of cards connected to it; a serial message bus connecting the cards across the midplane; a processor and bus interface on a first circuit board; and a control processor on each of the second circuit boards) relied upon in the rejection. Specifically, to construct the serial bus of Jobs with an open architecture that readily accommodates insertion of newly designed hardware and/or software (See Column 6 Lines 6-10 of Atkinson). The Examiner further notes that, as shown in the above rejection, the motivation provided to use Aggarwal teaches a benefit to using the features of Aggarwal (the routing engine) relied upon in the rejection. Specifically, to create a forwarding table allowing the device to determine the proper output port based on the destination address of incoming packets (See Column 6 Lines 4-48 of Aggarwal).

43. Applicant's arguments filed 12 February 2004 with respect to the rejection of Claims 11 and 12 over Jobs, Atkinson, and Aggarwal have been fully considered but they are not persuasive. Applicant has argued that Wong does not disclose the control logic recited in Claim 11. Wong teaches that a plurality of components, such as the switch of Jobs, can be connected to the primary bus, and that each component has a local controller (See Column 4 Lines 1-4).

44. Applicant's arguments filed 12 February 2004 with respect to the rejection of Claims 14 and 17 over Jobs, Atkinson, Aggarwal, and Simpson have been fully considered but they are not persuasive. Examiner notes that in the aforementioned rejections, Simpson is not being relied upon to teach elements of Claim 13.

45. Applicant's arguments filed 12 February 2004 with respect to the rejection of Claims 15 and 16 over Jobs, Atkinson, Aggarwal, Simpson, Li, and Baxter have been fully considered but they are not persuasive. Examiner notes that in the aforementioned rejections, Li and Baxter are not being relied upon to teach elements of Claim 14.

46. Applicant's arguments filed 12 February 2004 with respect to the rejection of Claims 18 and 19 over Atkinson, Posner, and Wong have been fully considered but they are not persuasive. Examiner notes that the switches of Posner, in addition to forming a complete link between an input and an output, also selectively connect and disconnect segments of the link (analogous to portions of the serial bus). Further, the switches of

Posner, when creating a link between two segments, selectively selects those segments, and when not creating a link between two segments, selectively disconnects those segments.

47. Applicant's arguments filed 12 February 2004 with respect to the rejection of Claim 22 over Atkinson, Posner, Wong, and Loftis have been fully considered but they are not persuasive. Examiner notes that in the aforementioned rejections, Loftis is not being relied upon to teach elements of Claim 18.

48. Applicant's arguments filed 12 February 2004 with respect to the rejection of Claim 24 over Atkinson, Posner, Wong, and Li have been fully considered but they are not persuasive. Examiner notes that in the aforementioned rejections, Li is not being relied upon to teach elements of Claim 18.

49. Applicant's arguments filed 12 February 2004 with respect to the rejection of Claim 25 over Atkinson, Posner, Wong, and Baxter have been fully considered but they are not persuasive. Examiner notes that in the aforementioned rejections, Baxter is not being relied upon to teach elements of Claim 18.

Conclusion

50. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (7-4:30), Alt. Fridays (7-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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